In The Claims:

Claim 1. (currently amended) A dynamic random access memory (DRAM) structure, comprising:

a substrate with a trench therein;

a capacitor formed inside the trench;

an active region surrounded by an isolation region formed over the substrate;

a word line formed over the substrate and passed through the active region, wherein an area in the active region covered by the word line serves as a channel region;

a pair of source/drain regions within the active region formed on each side of the word line such that the source/drain regions connect with the capacitor and a bit line respectively; and

a doped region with dopants in a conductive type identical to that of the substrate formed on each side of the channel region adjacent to the isolation region.

Claim 2. (original) The DRAM structure of claim 1, wherein the capacitor inside the trench comprises:

an external electrode in the substrate formed at a lower section of the trench;

a capacitor dielectric layer formed on the surface of the trench; and

a first conductive layer formed inside the trench and electrically connected to a corresponding source/drain region.

Claim 3. (original) The DRAM structure of claim 2, wherein the capacitor further comprises:

a collar dielectric layer formed on the sidewall above the first conductive layer;

and

a second conductive layer formed over the first conductive layer surrounded by the collar dielectric layer such that the first conductive layer connects electrically with a corresponding source/drain region through the first conductive layer.

Claim 4. (original) The DRAM structure of claim 3, wherein the capacitor further comprises a third conductive layer and a buried strap such that the third conductive layer is formed over the collar dielectric layer and the second conductive layer and is electrically connected to a corresponding source/drain region through the buried strap.

Claim 5. (original) The DRAM structure of claim 4, wherein the third conductive layer has a top surface below a top surface of the substrate.

Claim 6. (currently amended) A dynamic random access memory (DRAM) structure, comprising:

a substrate with a plurality of trenches therein;

a capacitor formed within each trench;

a plurality of active regions surround by an isolation region formed over the substrate;

a plurality of word lines running in a first direction formed over the substrate;

a plurality of source/drain regions and a plurality of common source/drain regions formed within various active regions such that a pair of source/drain region and a common source/drain region together form a group inside each active region;

a plurality of bit lines running in a second direction formed over the substrate; and

a plurality of doped regions formed in the substrate such that dopants inside the

doped region has a conductive type identical to that of the substrate,

wherein all four side edges of each active region have a pair of trenches such that the capacitor in one of the trenches in each pair of trenches along the second direction is coupled to the active region and the capacitors in the pair of trenches along the first direction are coupled to other active regions,

a pair of adjacent word lines passes through the active region and the two pairs of trenches along the first direction and the areas in the active region covered by the word lines serve as two channel regions, moreover, the doped regions are formed on each side of each channel region adjacent to the isolation region, and

each source/drain region within each active region is electrically connected to a capacitor and the common source/drain region is electrically connected to a bit line.

Claim 7. (original) The DRAM structure of claim 6, wherein the capacitor inside the trench comprises:

an external electrode in the substrate formed at a lower section of the trench;

a capacitor dielectric layer formed on the surface of the trench; and

a first conductive layer formed inside the trench and electrically connected to a corresponding source/drain region.

Claim 8. (original) The DRAM structure of claim 7, wherein the capacitor further comprises:

a collar dielectric layer formed on the sidewall of the trench above the first conductive layer; and

a second conductive layer formed over the first conductive layer surrounded by

the collar dielectric layer such that the first conductive layer connects electrically with a corresponding source/drain region through the first conductive layer.

Claim 9. (original) The DRAM structure of claim 8, wherein the capacitor further comprises a third conductive layer and a buried strap such that the third conductive layer is formed over the collar dielectric layer and the second conductive layer and is electrically connected to a corresponding source/drain region through the buried strap.

Claim 10. (original) The DRAM structure of claim 9, wherein the third conductive layer has a top surface below a top surface of the substrate.